A Scalable X86 CPU Design for 90nm Process

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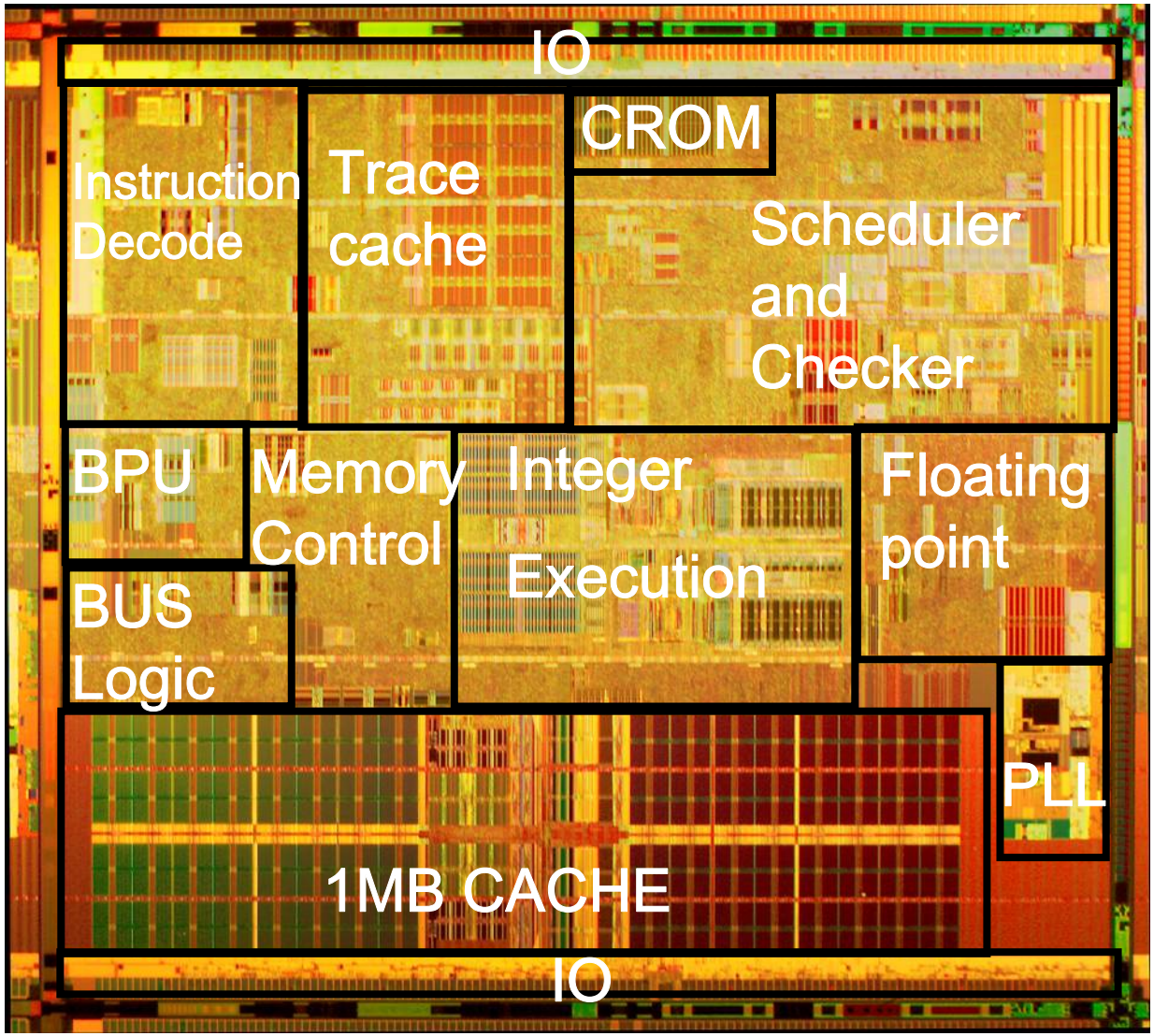
Features

- 4 Ghz Frequency
- Designed for 90nm technology
- Micro-Architecture Improvements
- 1MB Level 2 cache
- Designed to be scalable to as process improves
- Design Automation
- Design for Debug and Test
- New low voltage swing circuit technique
  - Session 8.3 at 9:30 AM Feb 17

90 nm X86 CPU

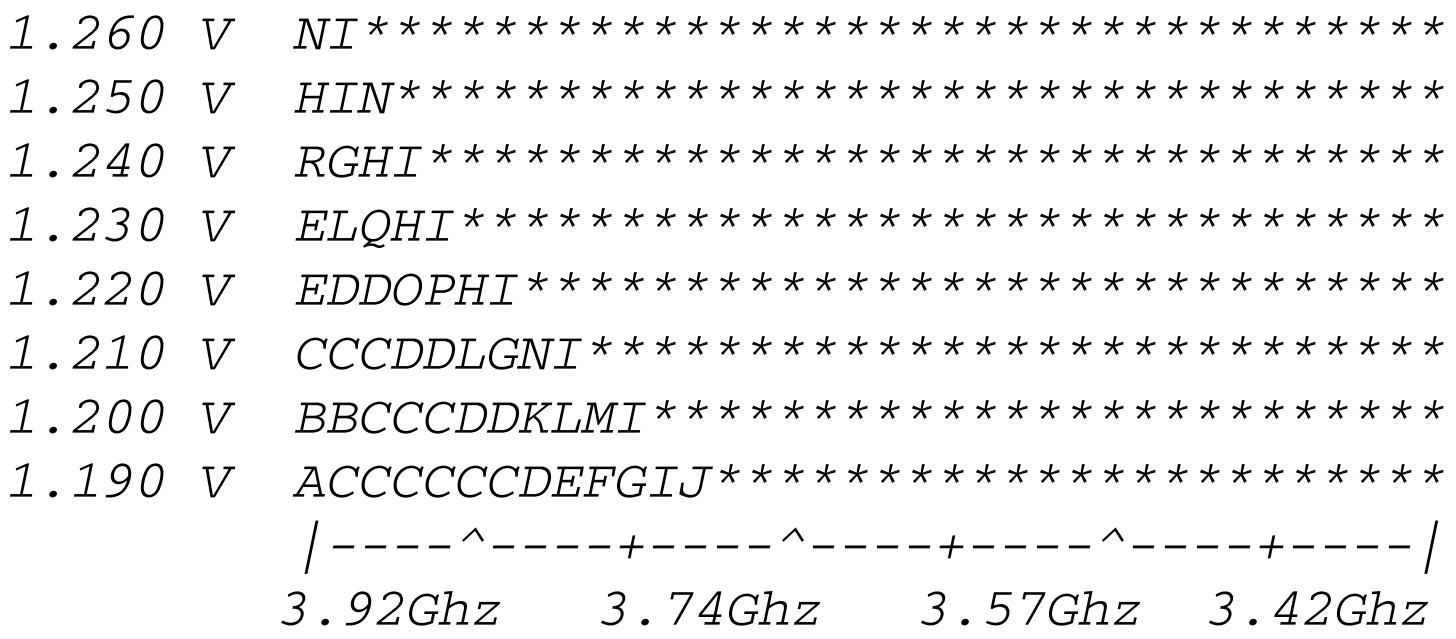


125 M Transistors

112 mm^2 Die Size

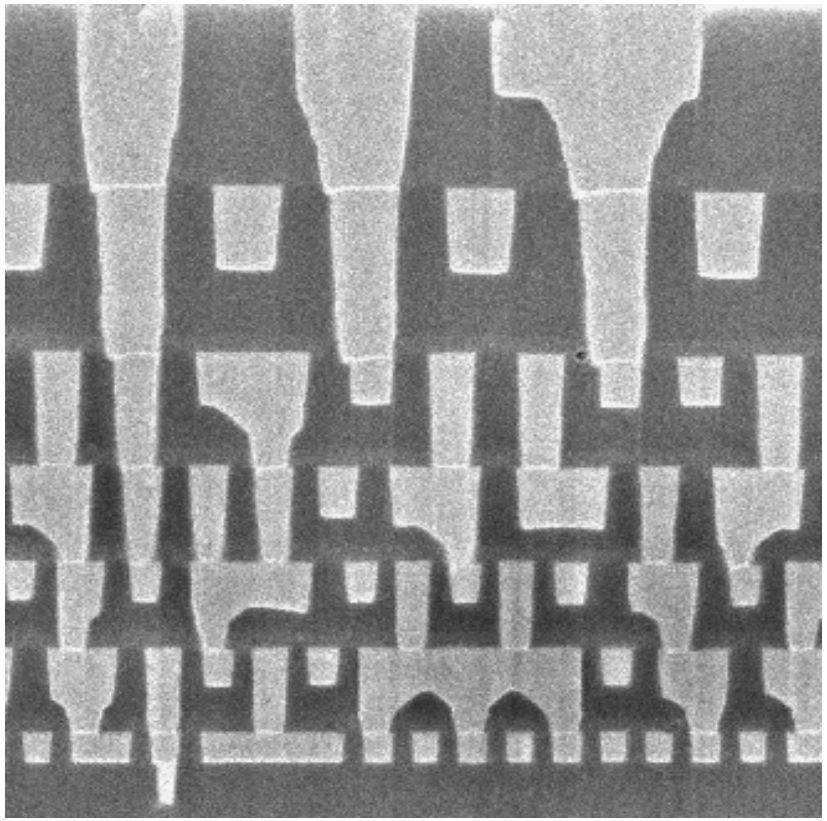
1.05u^2 SRAM bit

VCC vs. Frequency plot



Beginning of Life Clock Rate Met Expectations

Advanced 90nm Technology



M7

M6

M5

M4

M3

M2

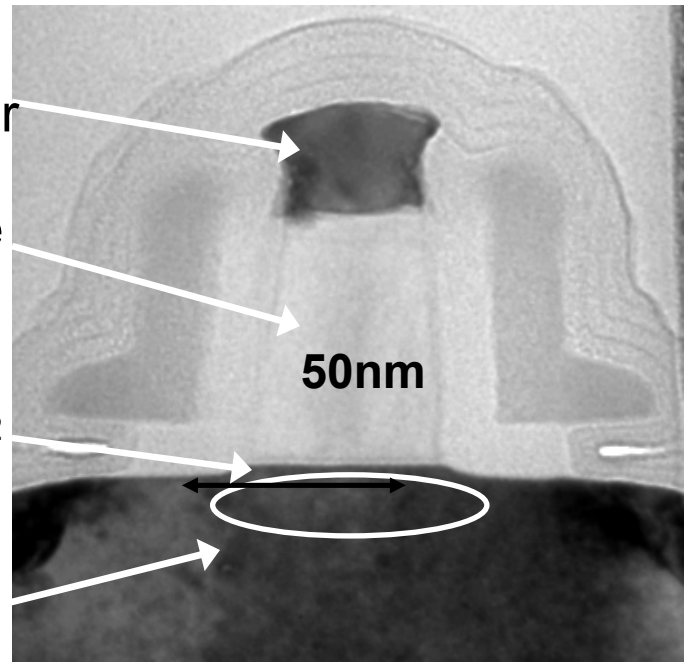
M1

Nickel Silicide Layer

Silicon Gate Electrode

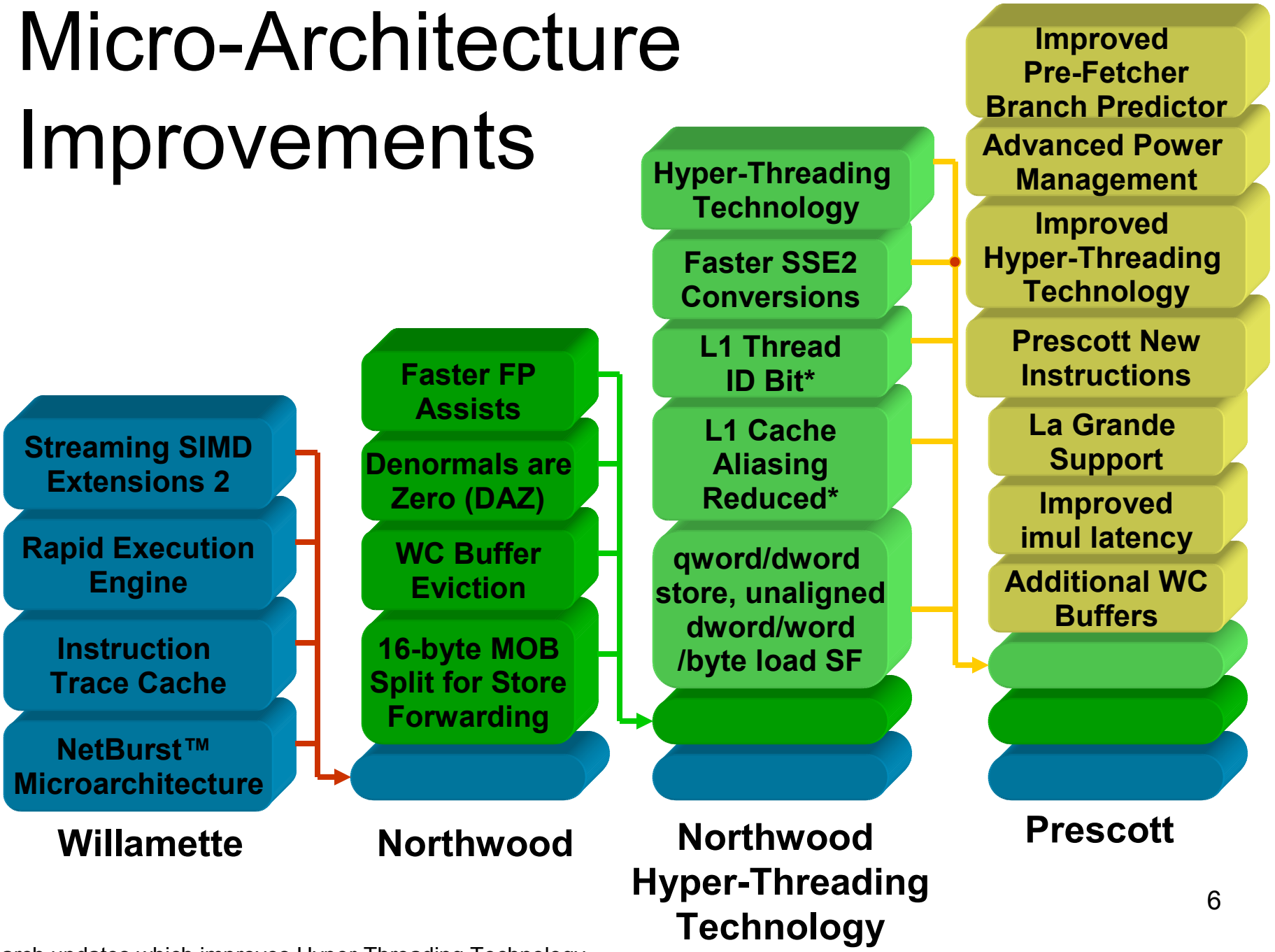
1.2 nm SiO_2 Gate Oxide

Strained Silicon



90nm Process with less than 50nm gate length on 300mm wafers

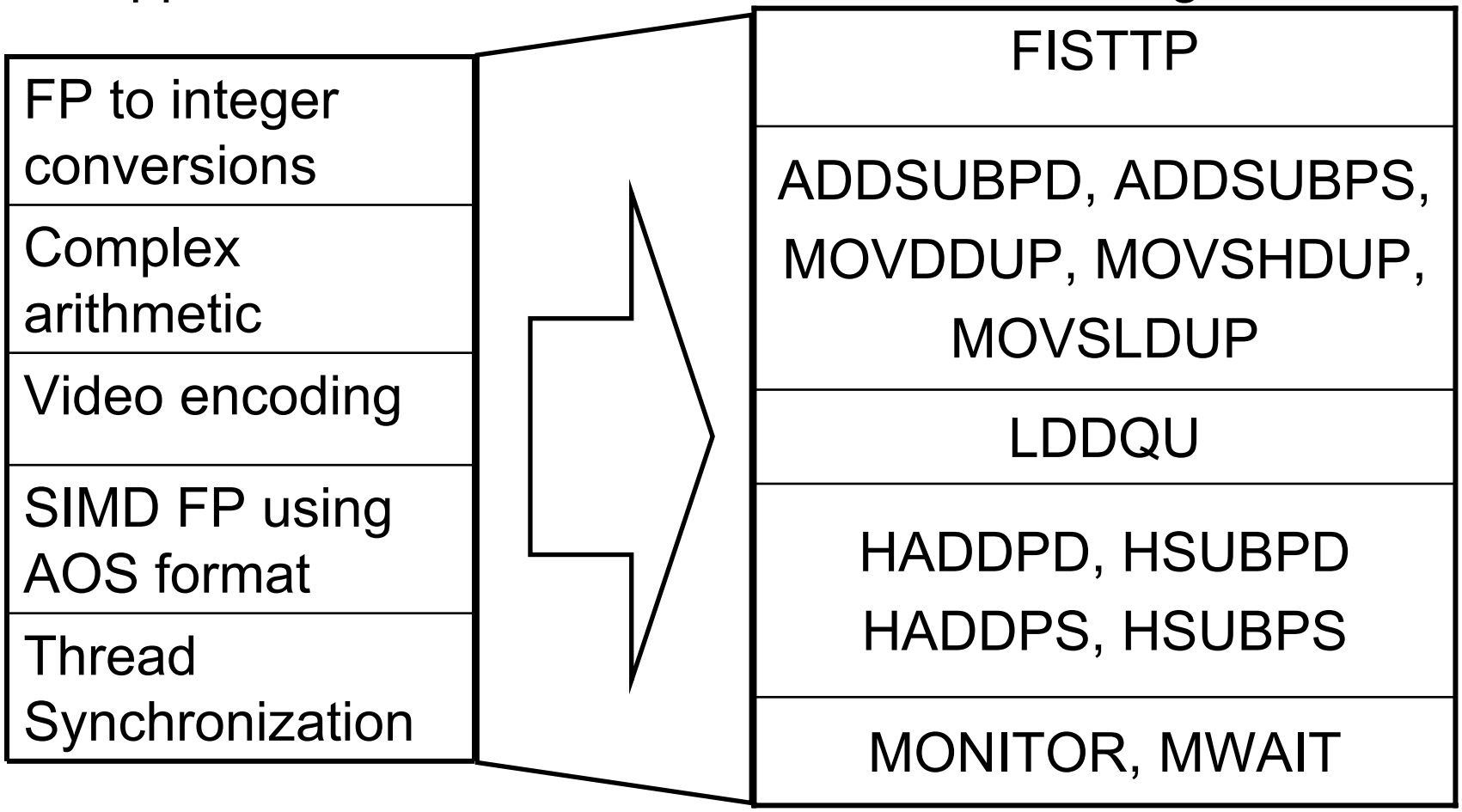
Micro-Architecture Improvements



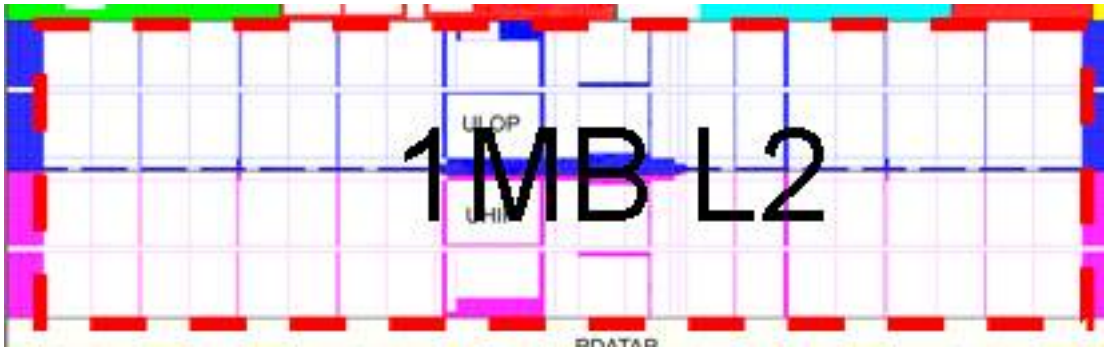
*u-arch updates which improves Hyper-Threading Technology

Prescott New Instructions

- 13 instructions added to improve specific application areas such as Media and Gaming



1MB 8way Set-Associative with ECC



- Maintain 2 cycle throughput through further bit line segmentation
  - Bit Cell that was optimized for low voltage operation ~10% larger
- 10.5 cycle latency
  - Re-pipelined for cycle time and array access latency optimization
- Enhanced Testability features
  - Programmable Built-in Self Test
  - Programmable Weak Write Test Mode
  - Low Yield Analysis circuits for defect analysis
  - Software Controlled Timing for improved post-silicon performance/timing optimization

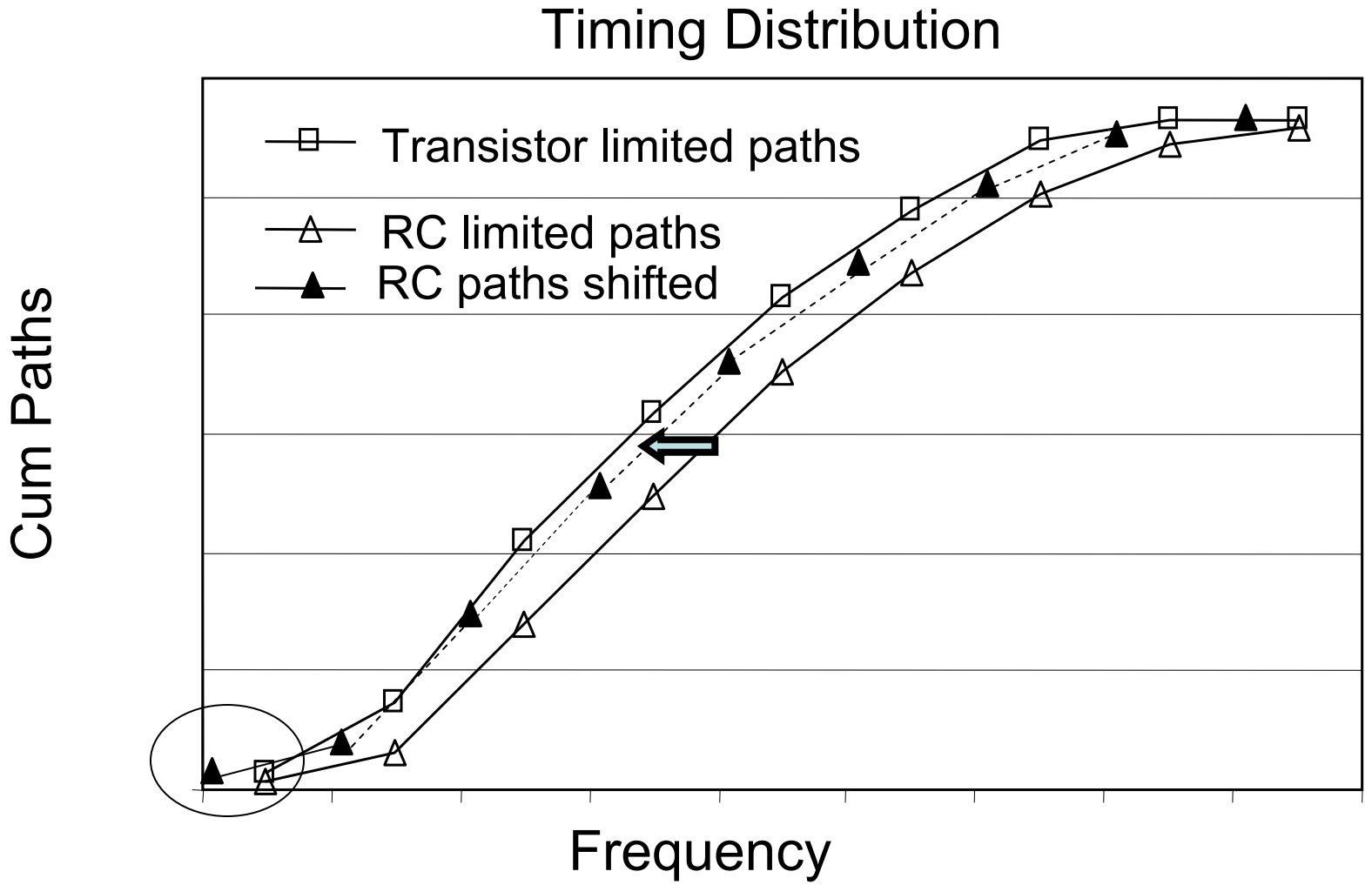
Design Issues for 90nm Technology

- RC management
- Clock Rate Scalability for the Life of the Process
- Leakage Management

RC Scalable Design

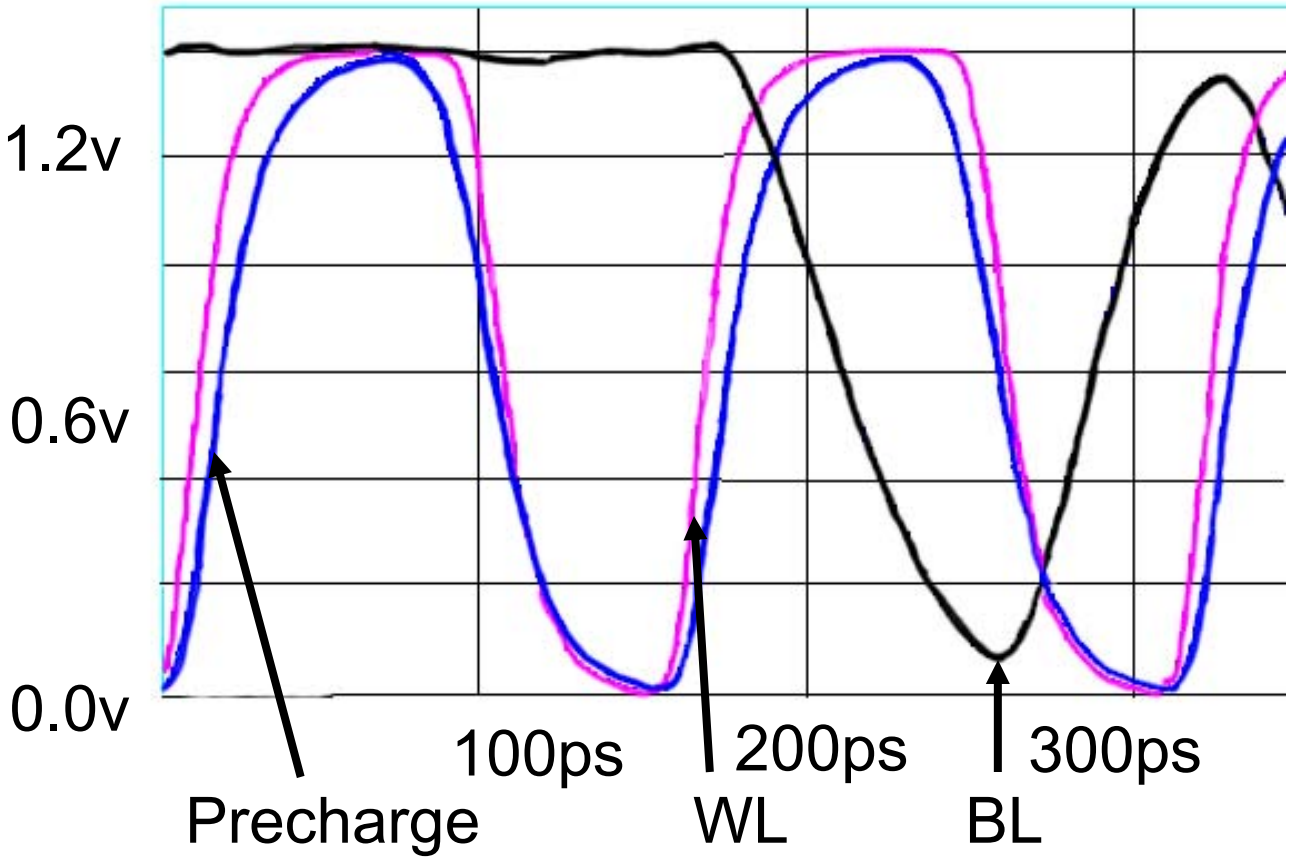
- Transistors increase in speed over process life
- Dual Design Constraints
  - Beginning of life transistor speed (BOL)
  - End of life transistor speed and RC's (EOL)
- Designing a scalable part required
  - Re-pipeling of multiple clock paths with large RC delays
  - Repeater spacing for process EOL
  - Designing arrays to be functional at EOL and BOL
  - Timing analysis to identify BOL and EOL paths
  - High frequency clock distribution for EOL
  - New circuit techniques in integer unit at EOL and BOL

Correct Management of RC's Minimizes Design Work



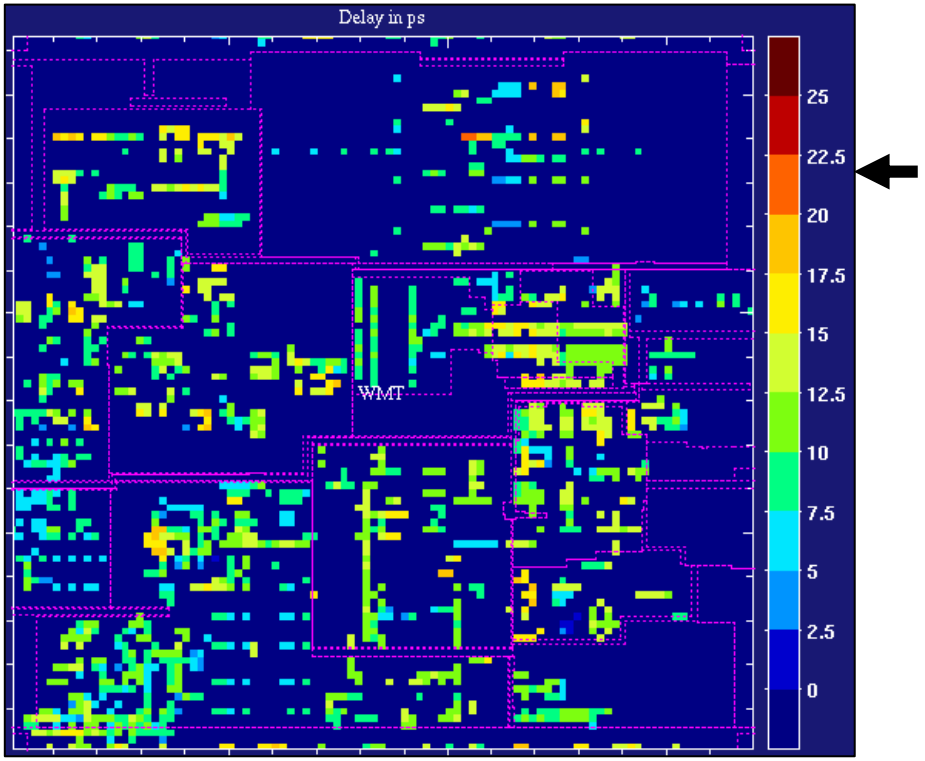
- Scaling of RCs allows end of life RC limited paths to appear worse in initial timing run

Register File waveforms

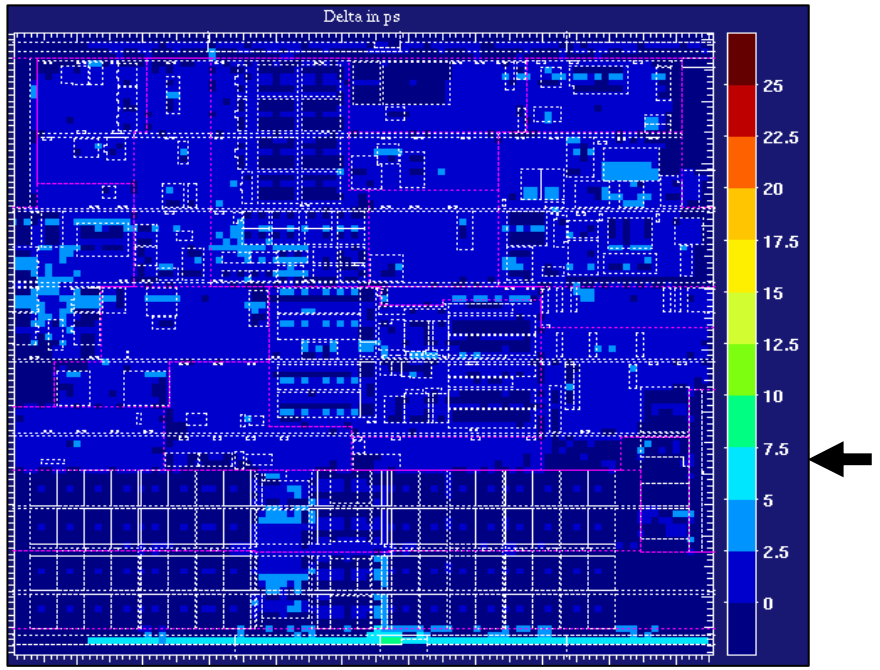


- Fast Rise and Fall Time for Wide Operating Margins at End of life Frequency

Improved Clock Distribution For Better Frequency Scaling



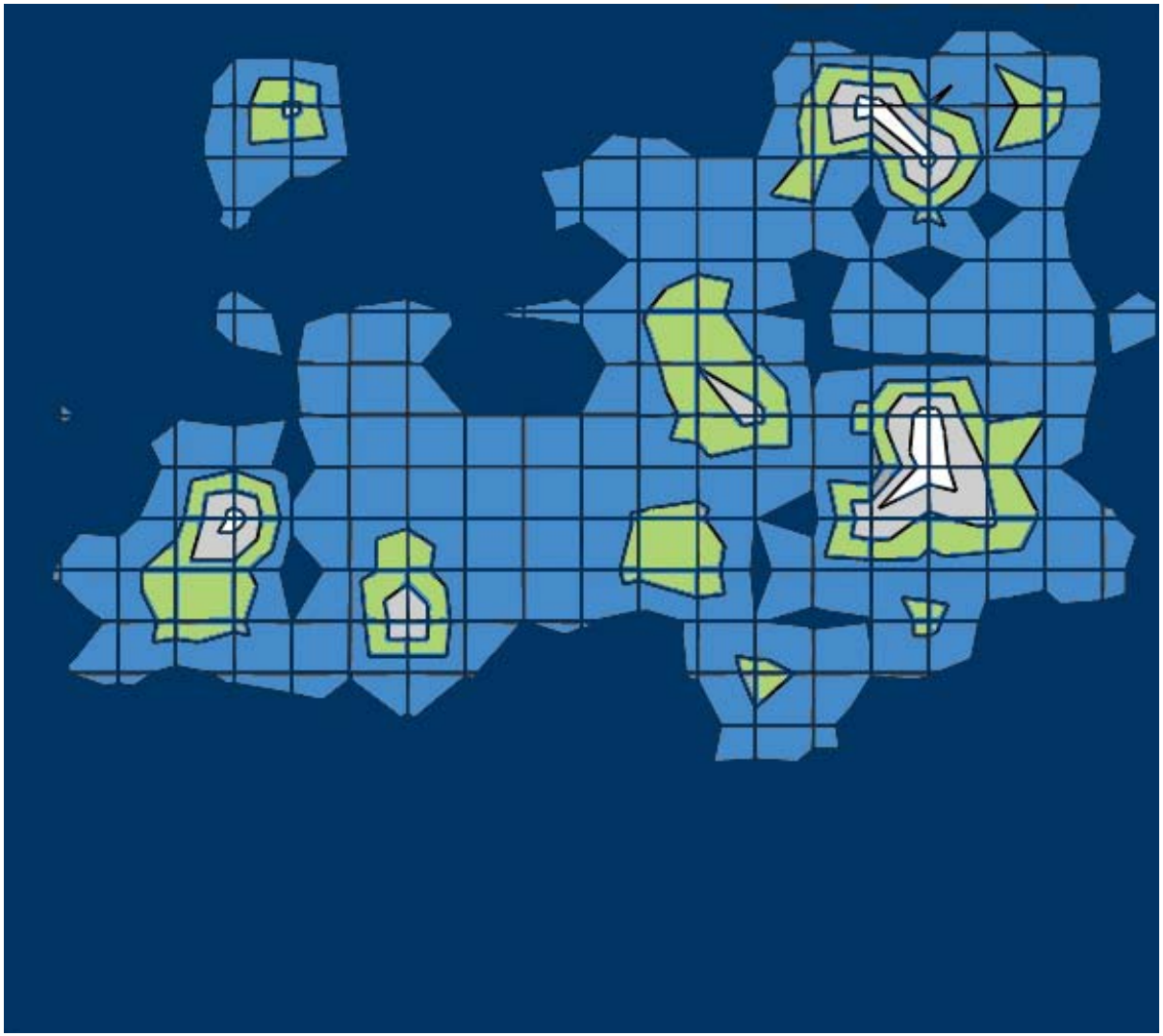
Northwood



Prescott

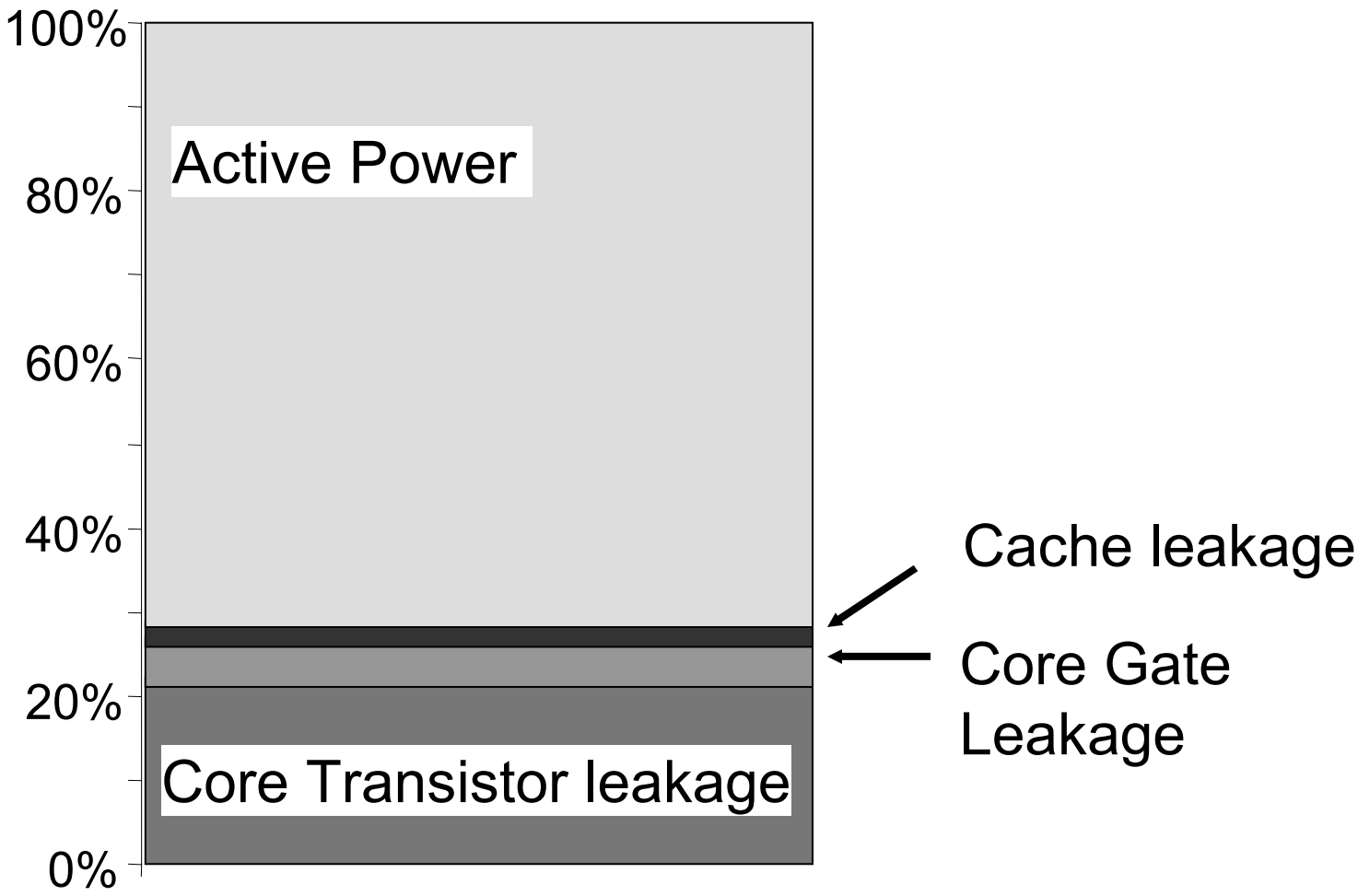
- Industry Leading Clocking Results
  - 4X better than Northwood
  - Skew less than one inverter
  - Power comparable to H-Tree

Die Temp Variation is Large



- RE Tools are temperature dependant
- Leakage tools also consider local temp

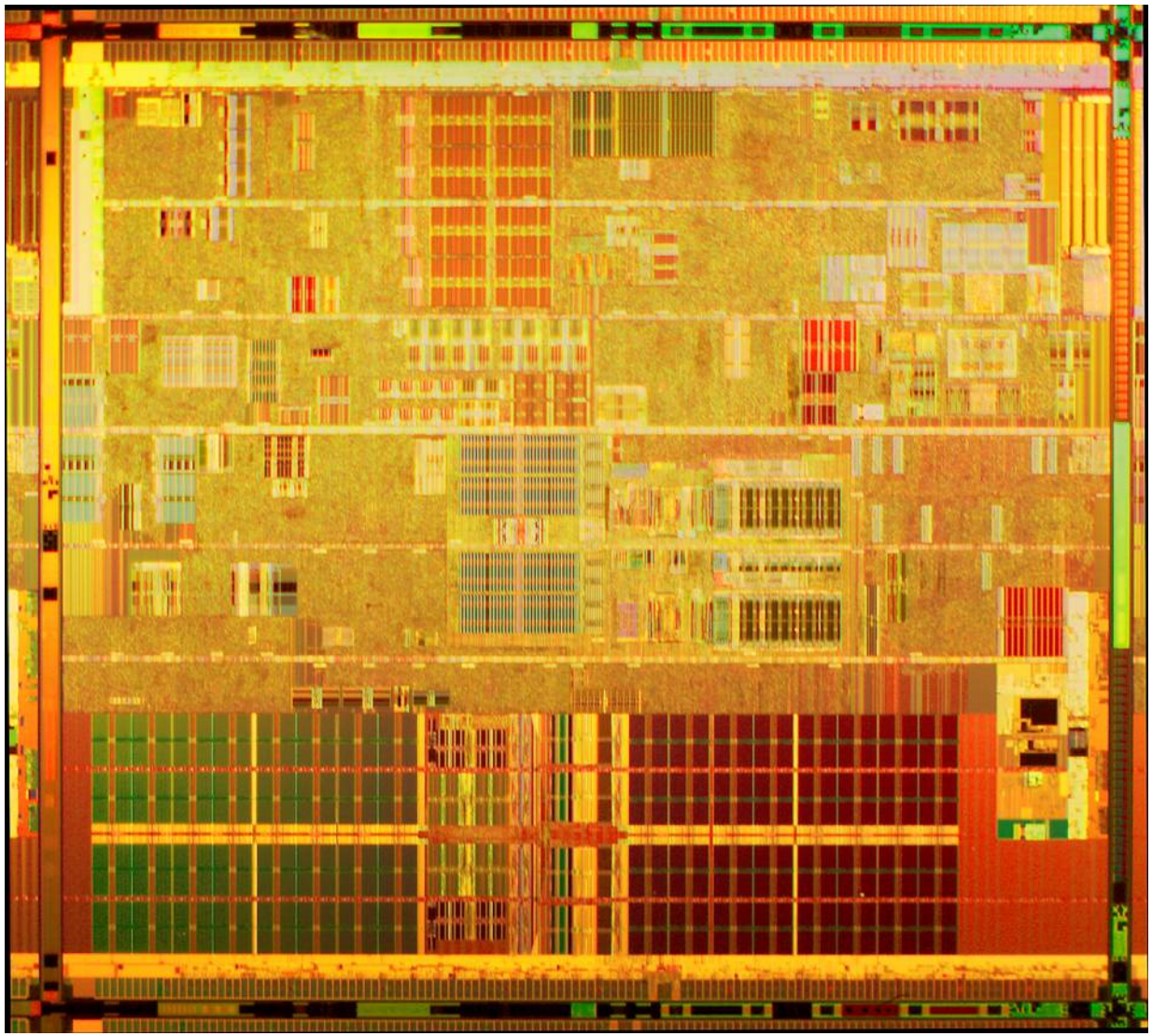
Leakage Management Results



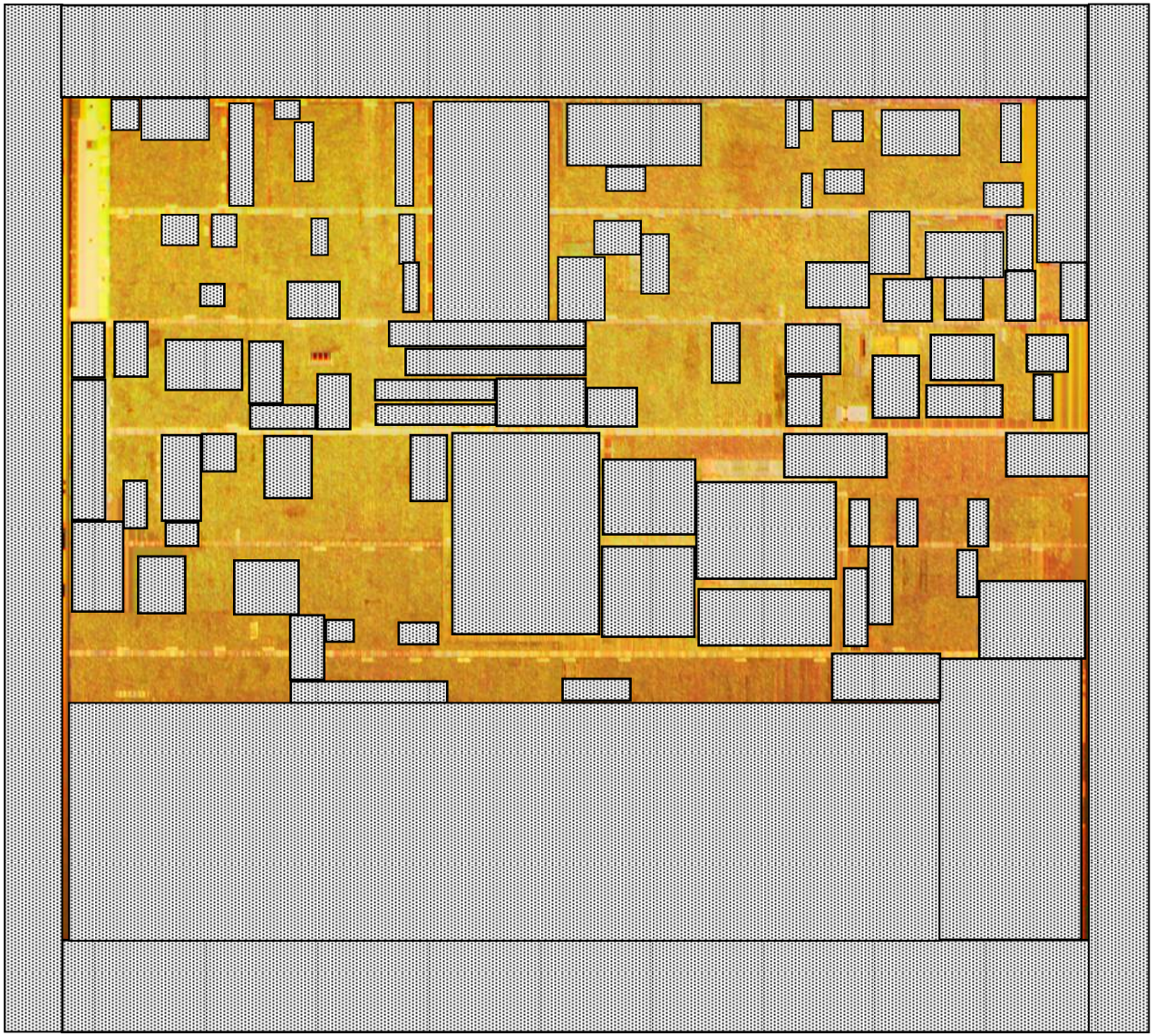
Design Automation

- Die Divided into 25 sections
- All layout and schematics hierarchies match sections
- Independent design of the sections
- Custom blocks and memory structures manually placed
- Random logic synthesized and auto placed
- All auto routed
- Clock tree synthesized
- Scan auto inserted

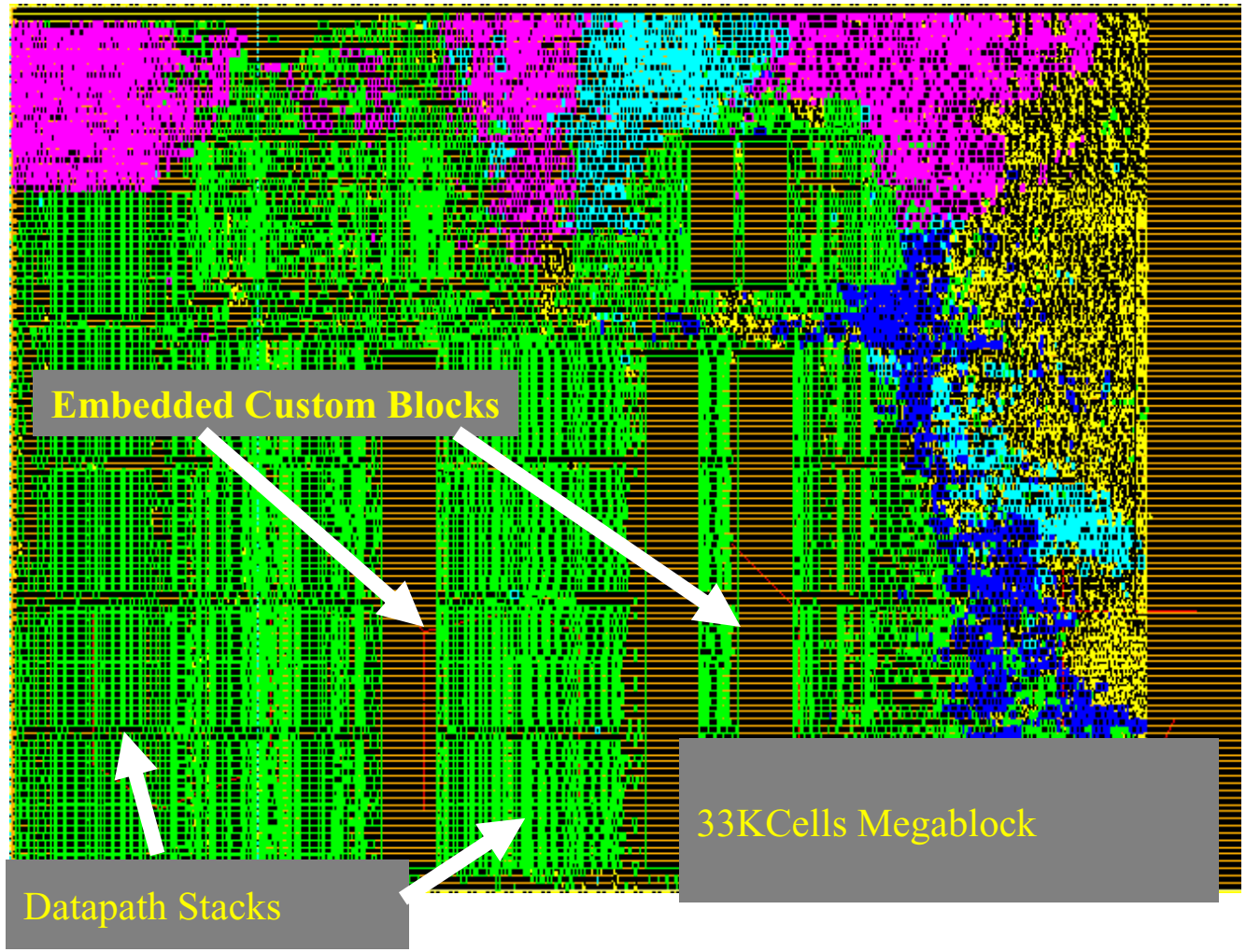
Die Photo



Die Photo with Regular Structures

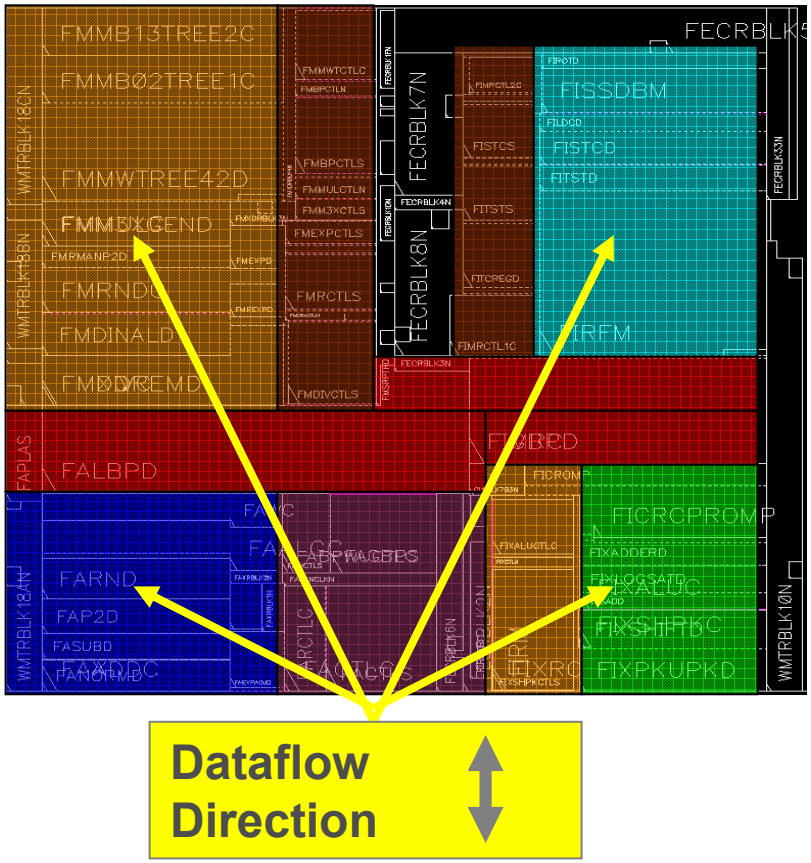


Better Placement Improves Clock Rate



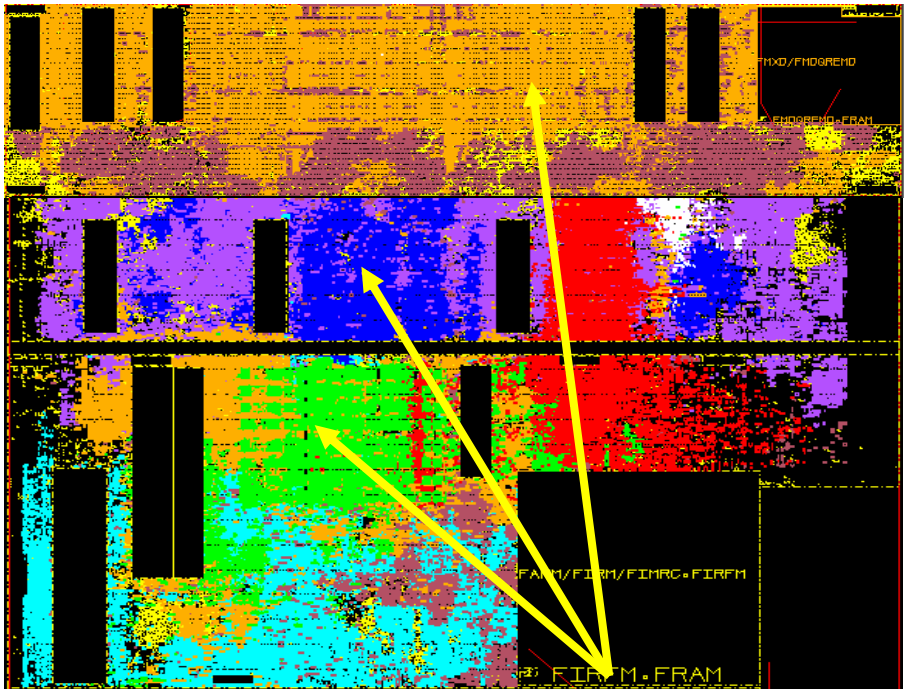
Automation Boosts Performance and Efficiency

Northwood Floating Point



Dataflow Direction

Prescott Floating Point



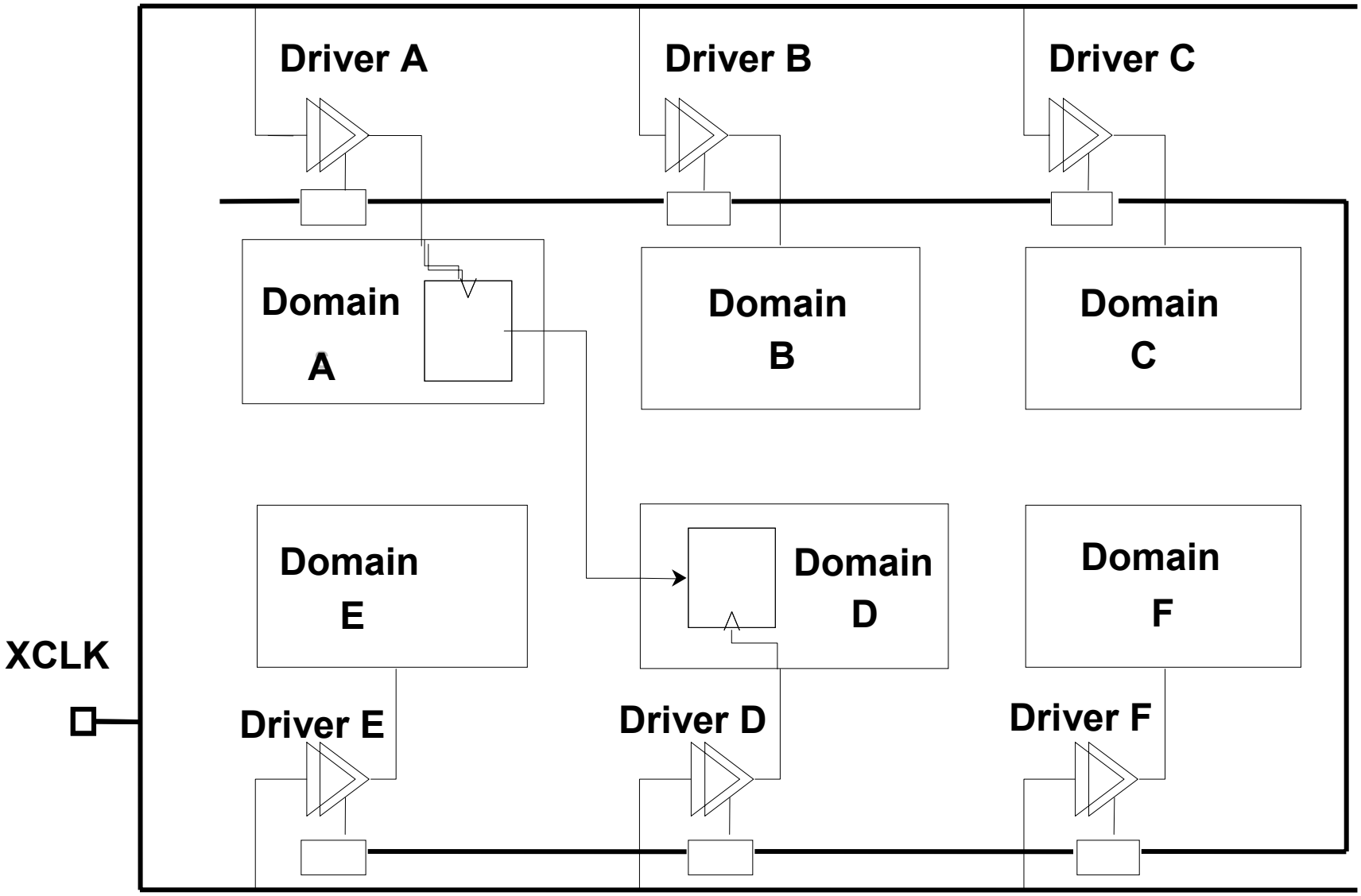
Dataflow Direction

- Superior Design Methods and Tools
  - Design completion through intelligent automation
  - Ease in building the top level chip
  - Faster design improvement with less resources

Design for debug and test

- Full Scan for all nodes
- Programmable BIST for caches
- Direct Access Test mode for other arrays
- Clock Timing Adjustment for debugging speed
- In die process monitors
- IO test modes

Clock Timing Adjustment



Summary

- Process scaleable 90 nm X86 processor achieved meeting performance goals
  - Advanced 7 metal process and strained transistors
  - Increased L2 cache to 1 Meg
- Micro-Architecture Improvements
- Process scaling did not impede design progress
  - RC's managed
  - Leakage within budget
  - Across die thermal variation accounted for
- Design automation used for half of the die area
  - Higher productivity and control
- Significant testability features added
- Speed debug enhanced with tune able clock network
- Clock rate will scale with transistor speed increases